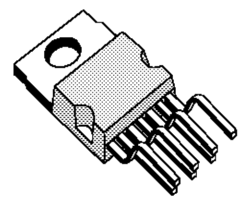
DUAL 5.1V REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES 5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8137

DESCRIPTION

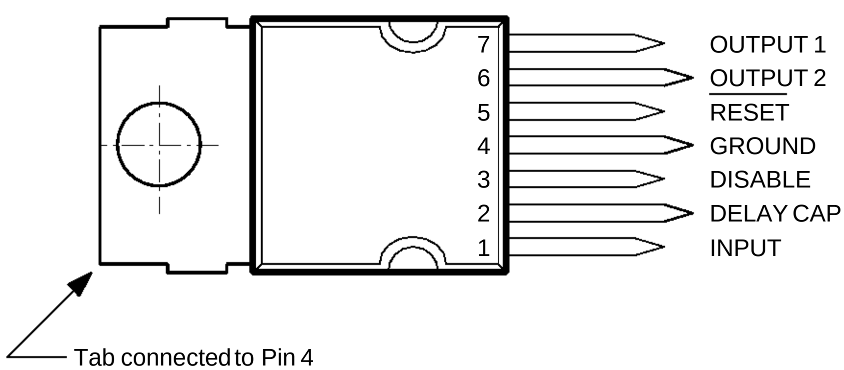
The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

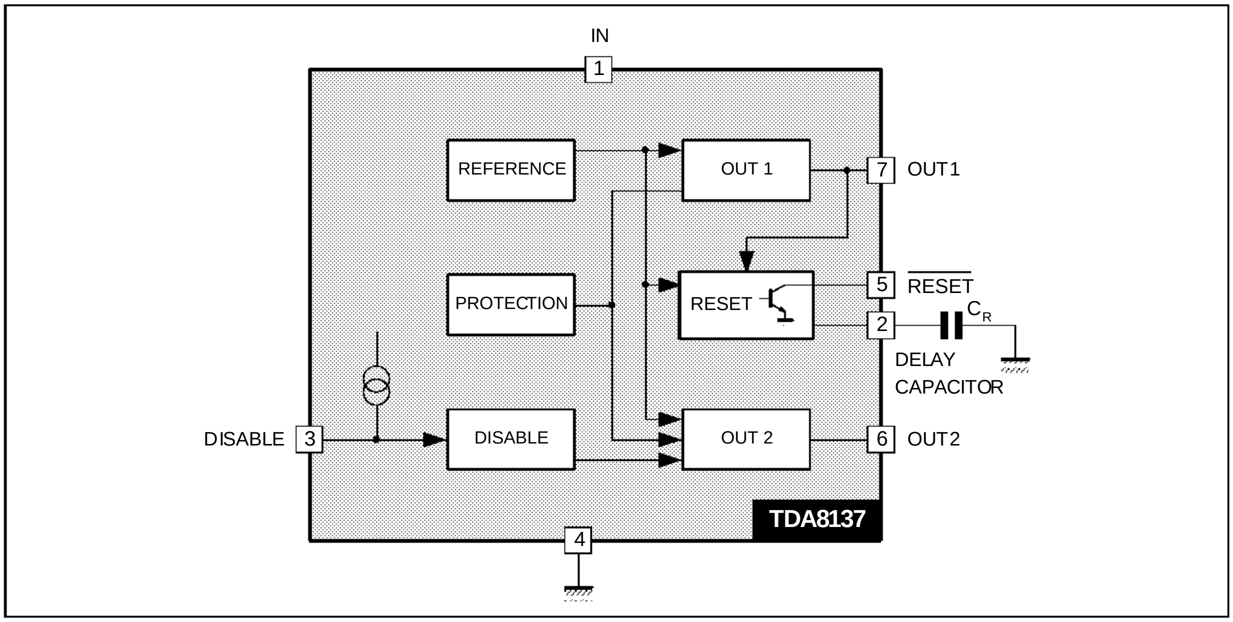
Short circuit and thermal protections are included.

PIN CONNECTION (top view)



8137-01.EPS

BLOCK DIAGRAM



8137-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at Pin 5	20	V
$I_{01,\ 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

8137-04.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W
T_j	Recommended Junction Temperature	Max.	0 to + 150	°C

8137-02.TBL

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{01,\ 2}$	Output Voltage	$I_{01,\ 2}$ = 10mA	5	5.1	5.2	V
		7V < V_{IN} < 14V, 5mA < I_0 < 750mA	4.9		5.3	V
$V_{I\ 01,\ 2}$	Dropout Voltage	$I_{01,\ 2}$ = 750mA			1.4	V
		$I_{01,\ 2}$ = 1A			2	V
$\Delta V_{01,\ 2LI}$	Line Regulation	7V < V_{IN} < 14V, $I_{01,\ 2}$ = 200mA			50	mV
$\Delta V_{01,\ 2LO}$	Load Regulation	5mA < $I_{01,\ 2}$ < 0.6A			100	mV
I_Q	Quiescent Current	I_{01} = 10mA, Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K–0.4	K–.25	K–0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see circuit description)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 5	C_e = 100nF (see circuit description)		25		ms
V_{RL}	Saturation Volt. at Pin 5 in Reset Condition	I_5 = 5mA			0.4	V

8137-03.TBL

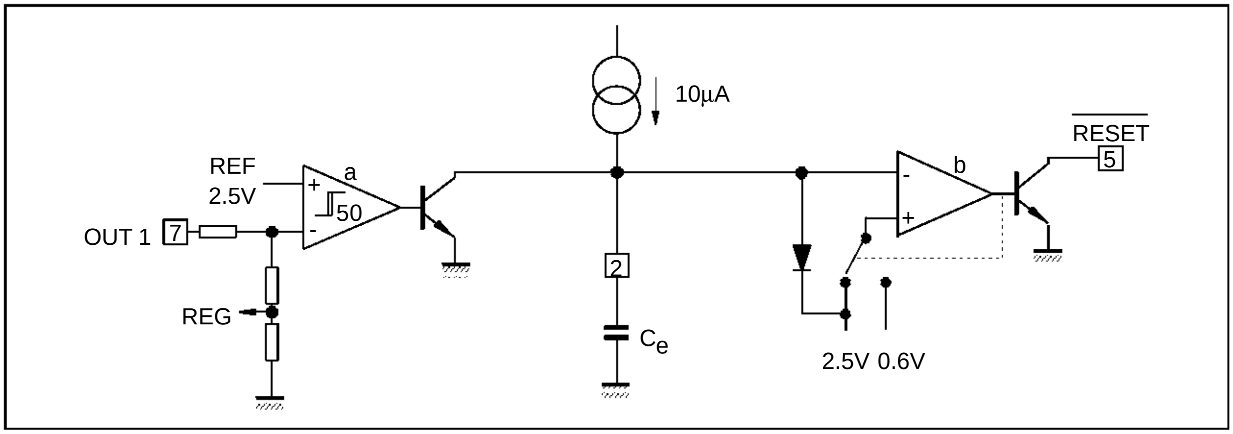
ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$K_{01,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta V_O \cdot 10^6}{\Delta T \cdot V_O}$ T_j = 0 to + 125°C		100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN} = 7V			1.6	A
		V_{IN} = 16V, (see note 1)			1	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 3	0V < V_{DIS} < 7V	-100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

8137-04.TBL

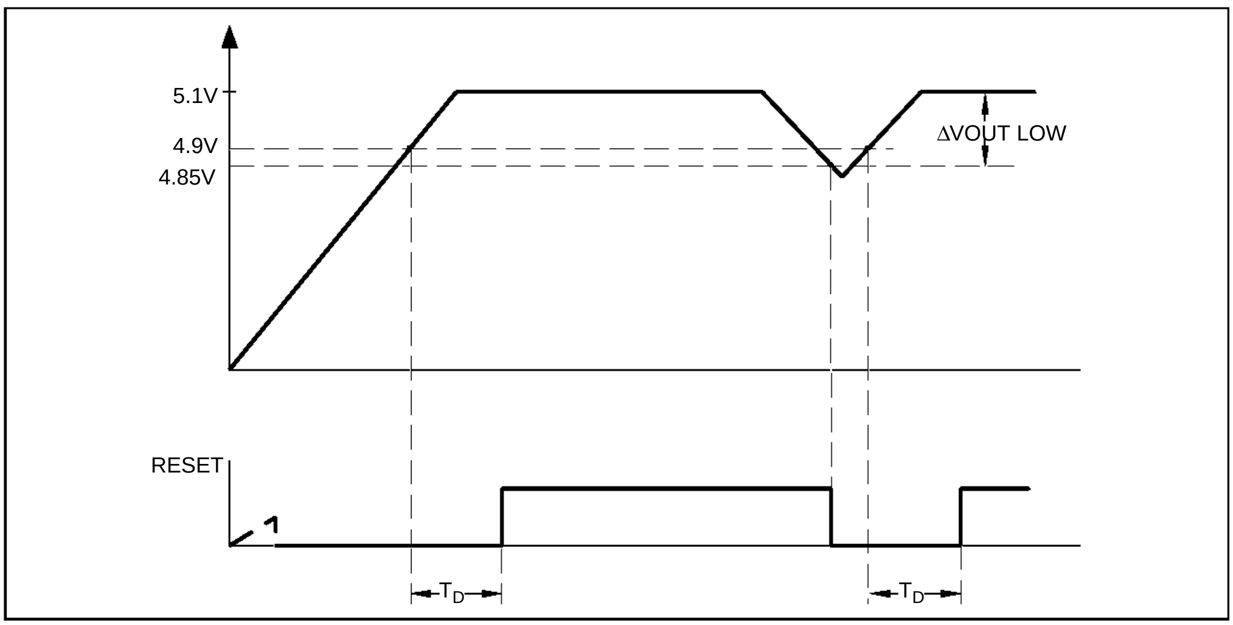
Note 1 : The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.
Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

Figure 1



8137-03.EPS

Figure 2



8137-04.EPS

CIRCUIT DESCRIPTION

The TDA8137 is a dual voltage regulator with Reset and Disable.

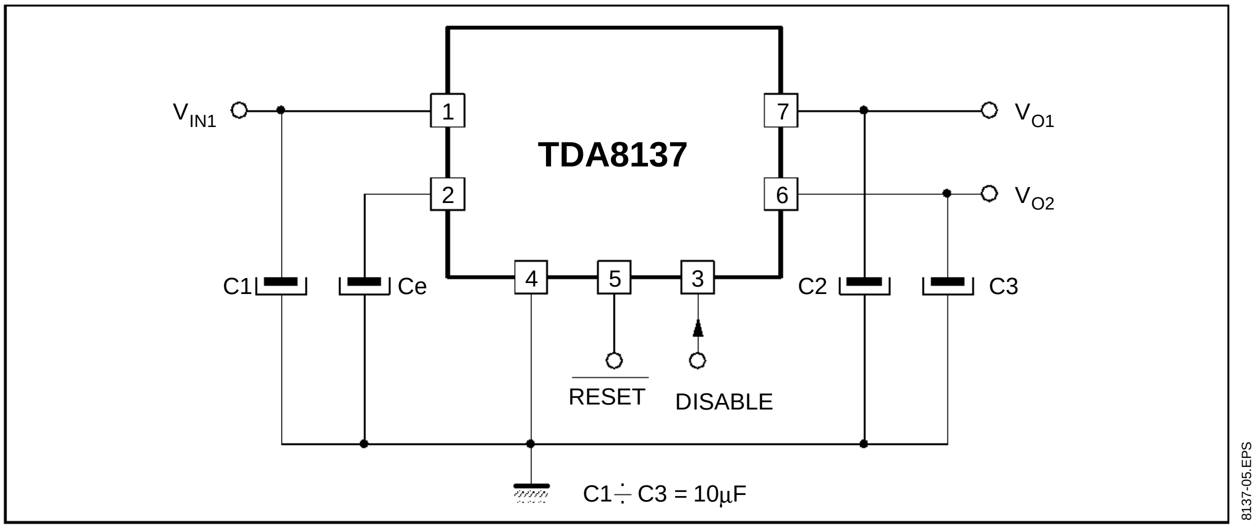
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

The outputs stages have been realized in darlington configuration with a drop typical of 1.2V.

The disable circuit, switches off the output 2 if a voltage lower than 0.8V is applied at pin 3.

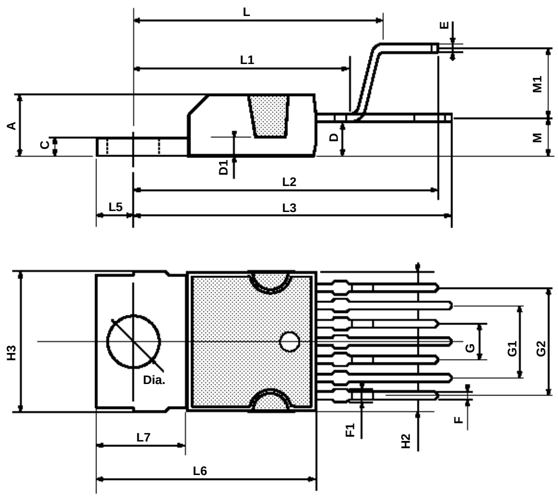
The Reset circuit checks the voltage at the output 1. If this one goes below V_{OUT} - 0.25V (4.85V Typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor Ce and the reset output goes at once low. When the voltage at the OUT 1 rises above V_{OUT} -0.2V (4.9V Typ.), the voltage V_{Ce} increases linearly to 2.5V corresponding to a delay t_d following the low : $t_d = \frac{Ce \cdot 2.5V}{10\mu A}$ (see figure 2), then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

9 PINS - PLASTIC HEPTAWATT



PM-HEPTV.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		08	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

HEPTV.TBL